WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a data memory circuit having divided several cache lines storing data, and several entries; and

a tag circuit connected to the data memory circuit,

the tag circuit having an array of an associative memory including: a memory cell circuit having several memory cells storing address corresponding to the data stored in the data memory circuit and divided several rows; and a comparator circuit comparing the address stored in the memory cell circuit with input address,

the comparator circuit comparing the address stored in divided several rows of the memory cell circuit with the input address concurrently in each of divided rows storing the address, and generating a cache hit/miss determination signal based on the comparative result of each row, the hit/miss determination signal being supplied to the data memory circuit.

2. The device according to claim 1, wherein access to the cache line of the data memory circuit is made by selecting the corresponding entry from divided several lines in accordance with index address.

3. The device according to claim 1, wherein when the address is written to the memory cell circuit of several rows of the tag circuit, write is carried out at several cycles.

4. The device according to claim 1, wherein the same column memory cell of the memory cells of several rows of the tag circuit is connected to a common write bit line.

5. The device according to claim 1, wherein the same column memory cell of the memory cells of several rows of the tag circuit is connected to a common read bit line.

6. The device according to claim 1, wherein the same column memory cell of the memory cells of several rows of the tag circuit is connected to common write and read bit lines.

7. The device according to claim 1, wherein a compare/determine operation of the comparator circuit is controlled according to a control signal.

8. The device according to claim 1, wherein the tag circuit is controlled so that address comparison is not made during data write to the data memory circuit.

9. The device according to claim 8, wherein the comparator circuit is controlled so that the compare/determine operation is not made during data write to the data memory circuit.

10. A semiconductor memory device comprising:

a data memory circuit having divided two cache lines storing data, and two entries; and

a tag circuit connected to the data memory circuit,

the tag circuit having an array of an associative memory including: a memory cell circuit having several memory cells storing address corresponding to the data stored in the data memory circuit and divided two rows; and a comparator circuit comparing the address stored in the memory cell circuit with input address,

the comparator circuit comparing the address stored in divided two rows of the memory cell circuit with the input address concurrently in each of divided two rows storing the address, and generating a cache hit/miss determination signal based on the comparative result of each row, the hit/miss determination signal being supplied to the data memory circuit.

11. The device according to claim 10, wherein access to the cache line of the data memory circuit is made by selecting the corresponding entry from divided two lines in accordance with index address.

12. The device according to claim 10, wherein when the address is written to the memory cell circuit of two rows of the tag circuit, write is carried out at several cycles.

13. The device according to claim 10, wherein the same column memory cell of the memory cells of several rows of the tag circuit is connected to a common write bit line.

14. The device according to claim 10, wherein the same column memory cell of the memory cells of two rows

of the tag circuit is connected to a common read bit line.

15. The device according to claim 10, wherein the same column memory cell of the memory cells of two rows of the tag circuit is connected to common write and read bit lines.

16. The device according to claim 10, wherein a compare/determine operation of the comparator circuit is controlled according to a control signal.

17. The device according to claim 10, wherein the tag circuit is controlled so that address comparison is not made during data write to the data memory circuit.

18. The device according to claim 17, wherein the comparator circuit is controlled so that the compare/determine operation is not made during data write to the data memory circuit.

19. A semiconductor memory device comprising:

a data memory circuit temporarily storing data; and

a tag circuit connected to the data memory circuit,

the tag circuit having an array of an associative memory including: a memory cell circuit having several memory cells storing address corresponding to the data stored in the data memory circuit and divided several rows; and a comparator circuit comparing the address stored in the memory cell circuit with input address,

the comparator circuit comparing the address stored in divided several rows of the memory cell circuit with the input address concurrently in each of divided rows storing the address, and generating a cache hit/miss determination signal based on the comparative result of each row, the hit/miss determination signal being supplied to the data memory circuit.

20. The device according to claim 19, wherein the same column memory cell of the memory cells of several rows of the tag circuit is connected in common to any of write and read bit lines, write bit line an d read bit line.